REMARKS

This is in response to the Final Office Action dated March 24, 2004, claims 1, 3-31, and 33-39 are pending. The Examiner's reconsideration of the objections and rejections is respectfully requested in view of the amendments and remarks.

The Examiner has maintained an objection to the Title of the Invention first made in the Office Action dated October 1, 2003. The Title of the Invention has been amended to be clearly commensurate with the claims. The Examiner's reconsideration of the objection is respectfully requested.

The specification has been amended to correct an informality in the paragraph beginning at page 9, line 1.

Claims 1, 4, 5, 10-19, 21-31, 34, and 35 have been rejected under 35 U.S.C. 102(b) as being anticipated by Katzman (U.S. Patent No. 3,737,871). The Examiner stated essentially that Katzman teaches all the limitations of claims 1, 4, 5, 10-19, 21-31, 34, and 35.

Claims 1 and 31 claim, *inter alia*, "replacing the stack references with references to processor-internal registers; and synchronizing an architected state between the processor-internal registers and a main memory of the computer processing system." Claim 12 recites, *inter alia*, "determining whether a load instruction references a location in a local stack using an architecturally defined register for accessing a stack location, wherein each processor comprises a respective local stack; determining whether a rename register exists for the references location in the local stack, when the load instruction references the location using the architecturally defined register; and replacing the reference to the location by a reference to the rename register, when the rename register exists." Claim 26 claims, *inter alia*, "determining whether a store

instruction references a location in a local stack using an architecturally defined register for accessing a stack location, wherein each processor comprises a respective local stack; allocating a rename register for the location, when the store instruction references the location using the architecturally defined register; and replacing the reference to the location by a reference to the rename register."

Referring to claims 1, 12, 26, and 31, Katzman teaches a stack register architecture that uses a stack management system with stack instructions (see col. 1 lines 62-65 and col. 4, lines 31-35). Katzman does not teach "replacing the stack references with references to processor-internal registers" as claimed in claims 1 and 31, or "replacing the reference to the location by a reference to the rename register", as claimed in claims 12 and 26. Katzman does not teach a replacement step. Katzman teaches references to the stack using operations including PUSH, POP, QUP, QDWN, MREG, Exchange and Duplicate (see col. 4, lines 31-35 and col. 7, lines 30-41). The operations of Katzman are dedicated stack operations (see col. 1 lines 62-65) and do not use replacement. The operations of Katzman already reference the TOS registers implicitly. Where an architecturally defined stack access method is used, essentially as claimed in claims 1, 12, 26, and 31, a replacement of a stack reference is used to reference the processor-internal registers. Katzman does not teach a replacement step to reference the TOS registers. Therefore, Katzman does not teach "replacing the stack references with references to processor-internal registers" as claimed in claims 1 and 31, or "replacing the reference to the location by a reference to the rename register", as claimed in claims 12 and 26. The Examiner's reconsideration of the rejection is respectfully requested.

Claims 12 and 26 are believed to be allowable for additional reasons. Katzman operates the stack registers with "specialized stack operations" (see col. 4, lines 31-35). The specialized

stack operations operate on the stack by definition. Thus, Katzman does not teach determining whether a load instruction references a location in a local stack using an architecturally defined register for accessing a stack location, as claimed in claim 12, or determining whether a store instruction references a location in a local stack, as claimed in claim 26 (Emphasis added). Because Katzman's operations are known by definition to reference the stack, there is no need to determine whether the operations reference the stack. Therefore, Katzman fails to teach all the limitations of claims 12 and 26.

Claims 1 and 31 have been amended to include the limitations of claims 2 and 32, respectively. Claims 2 and 32 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Katzman in view of Morris (see below).

Multiple cited prior art references must suggest the desirability of being combined, and the references must be viewed without the benefit of hindsight afforded by the disclosure. The Examiner has chosen a multitude of references, apparently in hindsight, to reject claims 1 and 6, however, each reference relates to an entirely different art, for example, Katzman teaches a bookkeeping scheme for keeping track of the order of the information in a stack register (see Abstract), and Morris teaches a method for performing load and store operations in a multiprocessor environment for protecting store operations without affecting load operations and visa versa (see col. 4, lines 3-6 and col. 7, lines 5-10). Given the different fields of the references, stack management and multi-processor synchronization, and the lack of a suggestion or motivation to combine the references, these references are not believed to be combinable. Therefore, reconsideration of the rejections is respectfully requested.

Assuming, arguendo, that the references are combinable, the combined teachings of Katzman and Morris fail to teach or suggest all the limitations of claims 1 and 31.

Katzman teaches a plurality of top-of-stack registers for a stack management system with dedicated instructions (see col. 1 lines 62-65). As suggested by the Examiner Katzman does not teach synchronizing an architected state between the processor-internal registers and a main memory of the computer processing system wherein said synchronizing step comprises the step of inserting in-order write operations for all of the stack references that are write stack references that in-order write operations are inserted for all of the stack references that are write stack references. The operations of Katzman are dedicated stack operations (see col. 1 lines 62-65), and therefore do not need replacement. The operations of Katzman already reference the TOS registers implicitly. Katzman does not teach replacement of stack references, thus, there is teaching of synchronizing an architected state between the processor-internal registers and a main memory of the computer processing system, essentially as claimed in claims 1 and 31. Therefore, Katzman fails to teach or suggest all the limitations of claims 1 and 31.

Morris teaches forced load and store operations (see col. 5, lines 21-24). Morris does not teach or suggest, "synchronizing an architected state between the processor-internal registers and a main memory of the computer processing system" as claimed in claims 1 and 31. Morris teaches that the load and store operations can be executed without synchronization problems between CPUs (see col. 7, lines 5-10). Morris teaches synchronization between CPUs. Nowhere does Morris teach or suggest synchronization between processor-internal registers and a main memory, essentially as claimed in claims 1 and 31. Therefore, Morris fails to cure the deficiencies of Katzman.

The combined teachings of Katzman and Morris fail to teach or suggest "synchronizing an architected state between the processor-internal registers and a main memory of the computer

processing system" as claimed in claims 1 and 31. The Examiner's reconsideration of the rejection is respectfully requested.

Claims 4, 5, 10, and 11 depend from claim 1. Claims 13-19 and 21-25 depend from claims 12. Claims 27-30 depend from claim 26. Claims 34 and 35 depend from claims 31. The dependent claims are believed to be allowable for at least the reasons given for the independent claims. Reconsideration of the rejection is respectfully requested.

Claims 2-3, 32-33, and 36 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Katzman in view of Morris et al., (U.S. Patent No. 6,286,095). The Examiner stated essentially that the combined teachings of Katzman and Morris teach or suggest all the limitations of claims 2-3, 32-33, and 36.

Claims 2-3, and 32-33 have been cancelled. Claim 36 depends from claim 31. The dependent claim is believed to be allowable for at least the reasons given for claim 31. Reconsideration of the rejection is respectfully requested.

Claims 6, 8, 9, 20, and 39 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Katzman, in view of Wing (U.S. Patent No. 5,926,832). The Examiner stated essentially that the combined teachings of Katzman and Wing teach or suggest all the limitations of claims 6, 8, 9, 20, and 39.

Claims 6, 8, and 9 depend from claim 1. Claim 20 depends from claim 12. Claim 39 depends from claims 31. The dependent claims are believed to be allowable for at least the reasons given for claims 1, 12, and 31. Reconsideration of the rejection is respectfully requested.

Claims 7, 37, and 38 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Katzman, in view of Wing and Morris et al. (U.S. Patent No. 6,286,095). The Examiner

stated essentially that the combined teachings of Katzman, Wing, and Morris teach or suggest all the limitations of claims 7, 37, and 38.

Claim 7 depends from claim 1. Claims 37 and 38 depend from claim 31. The dependent claims are believed to be allowable for at least the reasons given for claims 1 and 31. At least claims 7 and 37 are believed to be allowable for additional reasons.

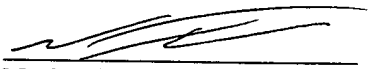
Claims 7 and 39 claim, "wherein the in-order value is written to the main memory by an in-order write operation inserted into an instruction stream containing an instruction corresponding to the stack reference, when the stack reference is a write stack reference."

As suggested by the Examiner, Katzman, in combination with Wing, have not taught wherein the in-order value is written to the main memory by an in-order write operation inserted into an instruction stream containing an instruction corresponding to the stack reference, when the stack reference is a write stack reference.

Morris teaches forced load and store operations (see col. 5, lines 21-24). Morris does not teach or suggest "wherein the in-order value is written to the main memory by an in-order write operation inserted into an instruction stream containing an instruction corresponding to the stack reference, when the stack reference is a write stack reference" as claimed in claims 7 and 37. Morris teaches that the load and store operations can be executed without synchronization problems between CPUs (see col. 7, lines 5-10). Morris teaches synchronization between CPUs. Nowhere does Morris teach or suggest synchronization between processor-internal registers and a main memory, essentially as claimed in claims 1 and 31. Further, Morris teaches only load and store operations and does not teach or suggest inserting in-order write operations for all of the stack references, essentially as claimed in claims 1 and 31. Therefore, Morris fails to cure the deficiencies of Katzman and Wing. Reconsideration of the rejection is respectfully requested.

Accordingly, claims 1, 3-31, and 33-39 are believed to be allowable for at least the reasons stated. The Examiner's withdrawal of the rejections is respectfully requested. For the forgoing reasons, the application is believed to be in condition for allowance. Early and favorable reconsideration is respectfully requested.

Respectfully submitted,



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